FIG_1

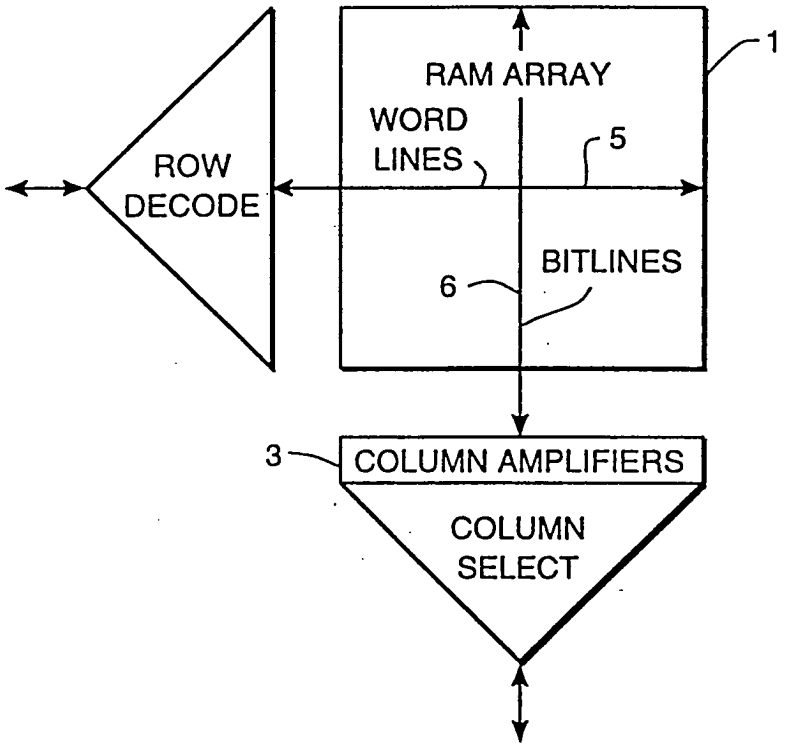

RAM ARRAY
1
WORD
LINES
5
ROW
DECODE
BITLINES
6
3
COLUMN AMPLIFIERS
COLUMN
SELECT

FIG_2

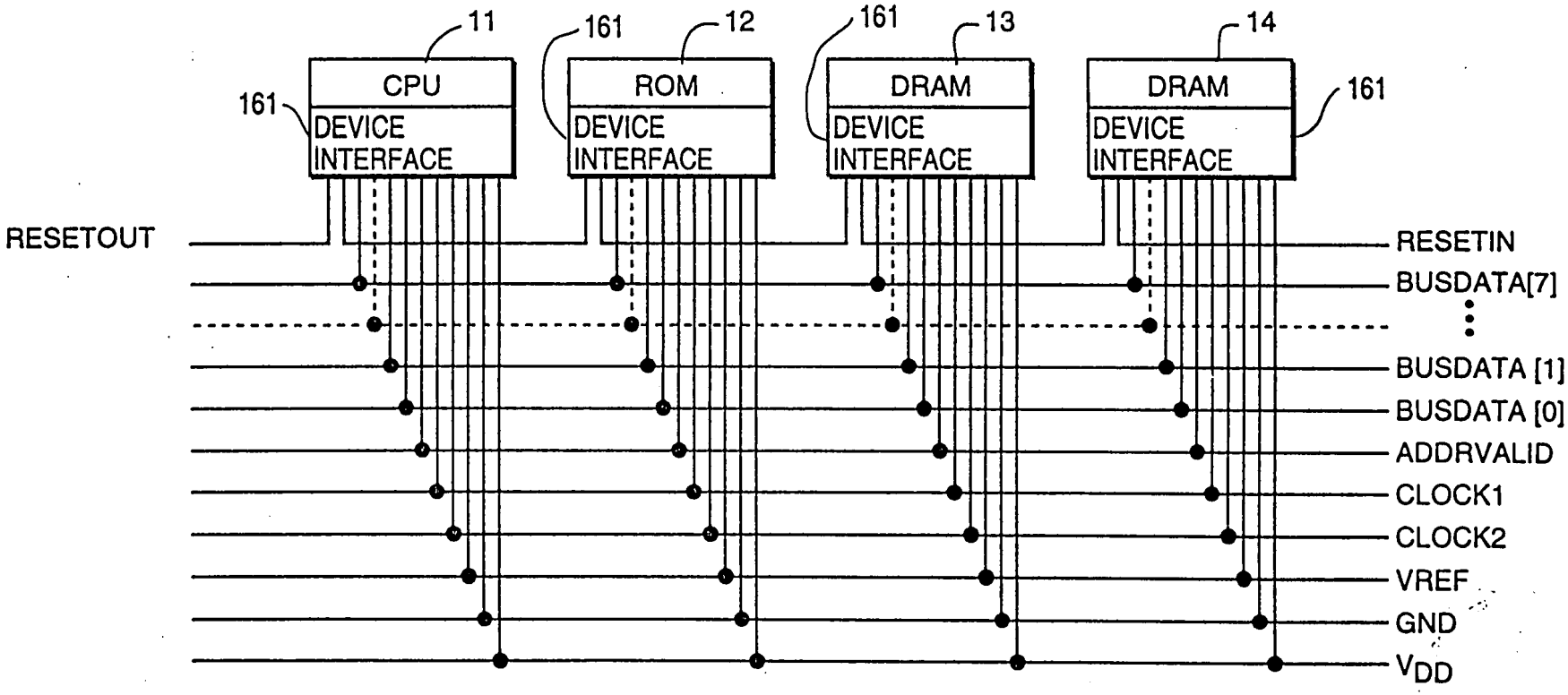
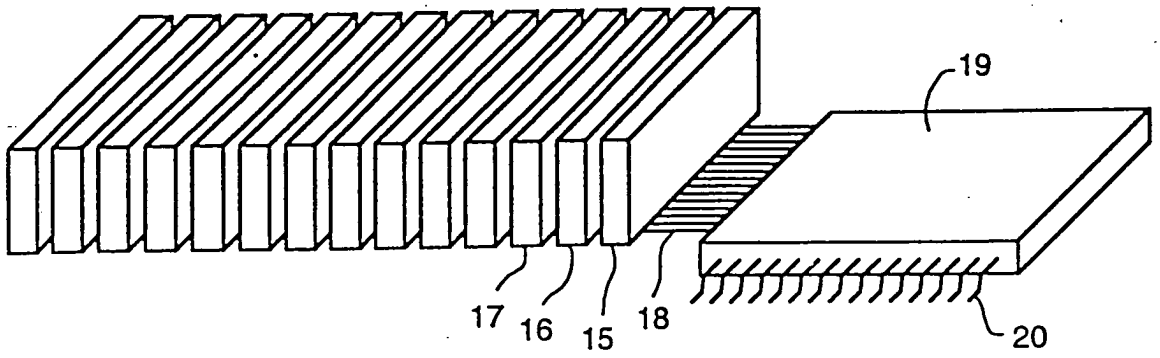

11
161
12
161
13
14
161
161
CPU
ROM
DRAM
DRAM
DEVICE INTERFACE
DEVICE INTERFACE
DEVICE INTERFACE
DEVICE INTERFACE
RESETOUT
RESETIN
BUSDATA[7]
BUSDATA [1]
BUSDATA [0]
ADDRVALID
CLOCK1
CLOCK2
VREF
GND
V_{DD}

FIG_3



REGULAR ACCESS

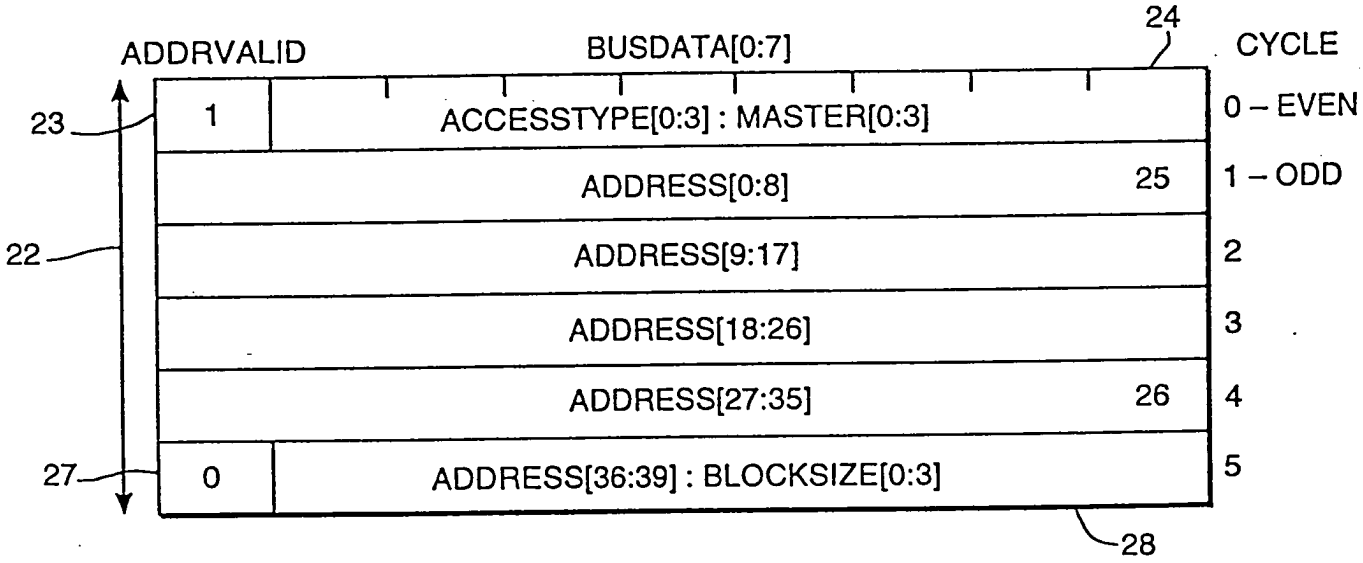


FIG_4

REJECT (NACK) CONTROL PACKET

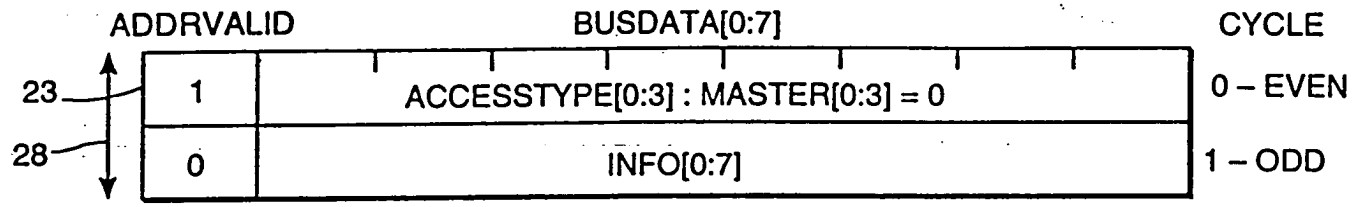


FIG_5

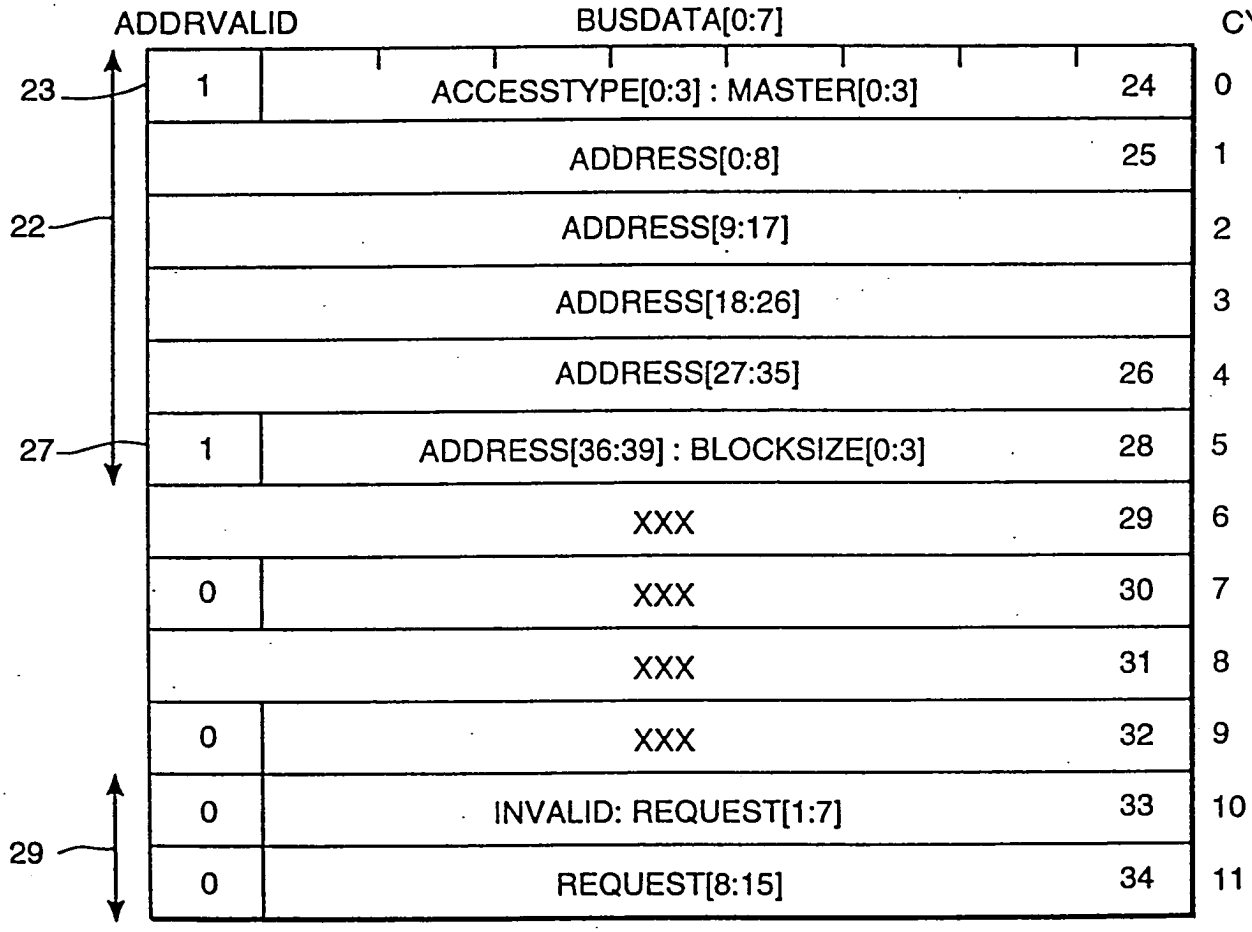


FIG_6

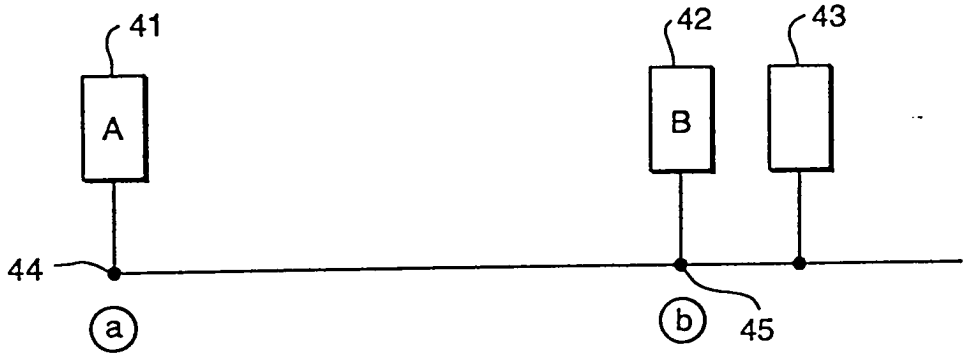


FIG_7A

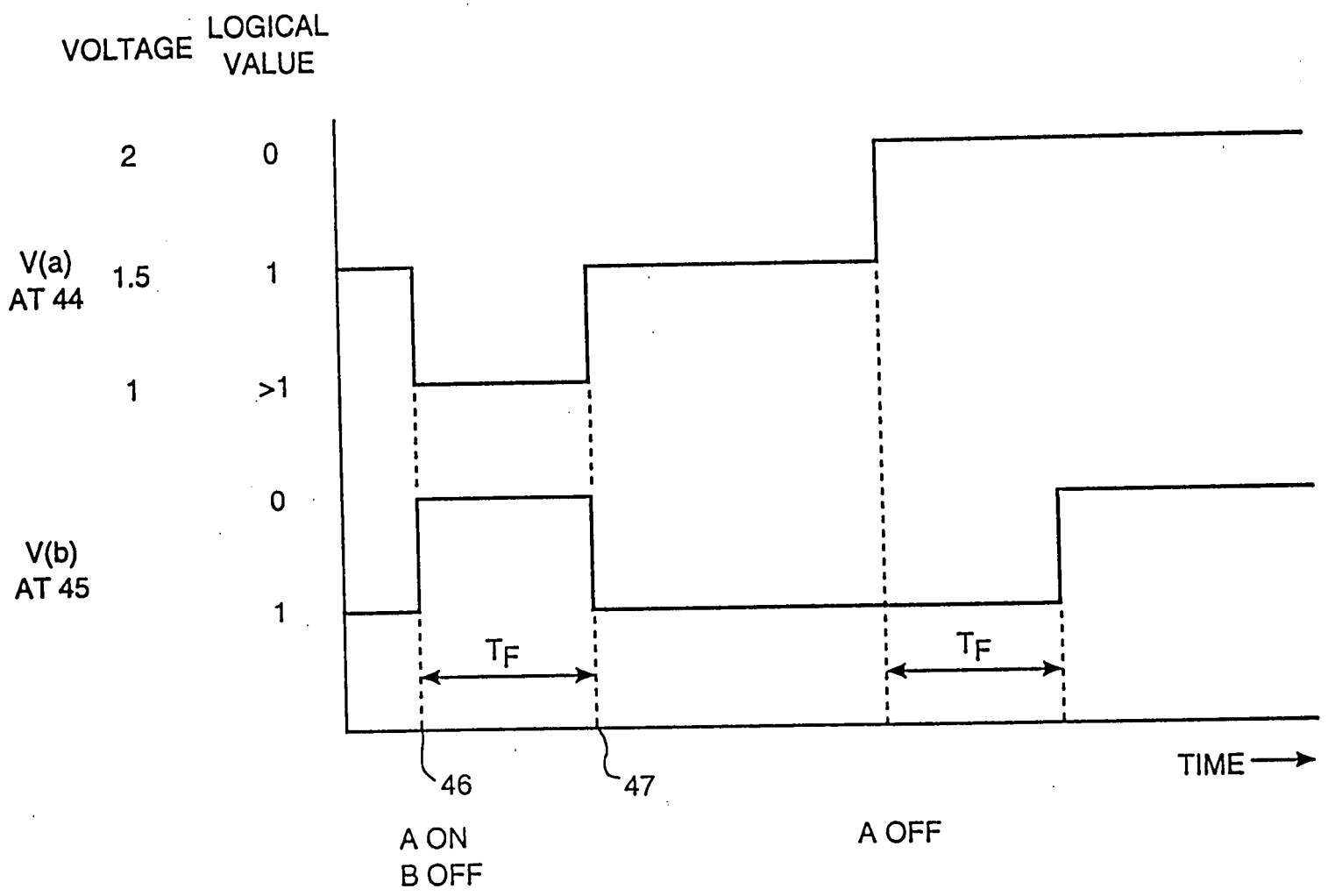

VOLTAGE
LOGICAL VALUE
2
0
V(a) AT 44
1.5
1
1
>1
0
V(b) AT 45
1
T_F
T_F
TIME
46
47
A ON
B OFF
A OFF

FIG_7B

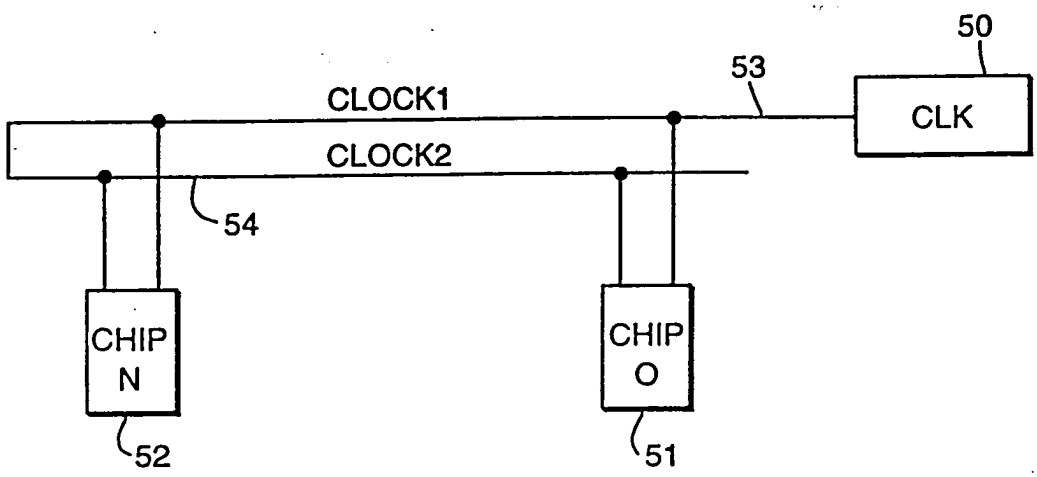

50
53
CLOCK1
CLK
CLOCK2
54
CHIP N
CHIP O
52
51

FIG_8A

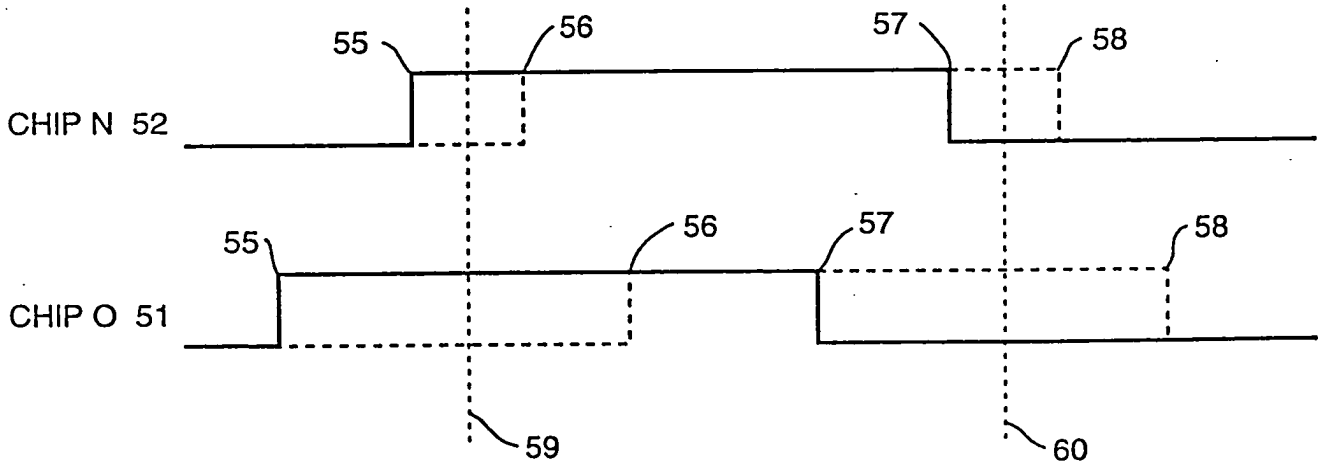

55
56
57
58
CHIP N 52
55
56
57
58
CHIP O 51
59
60

FIG_8B

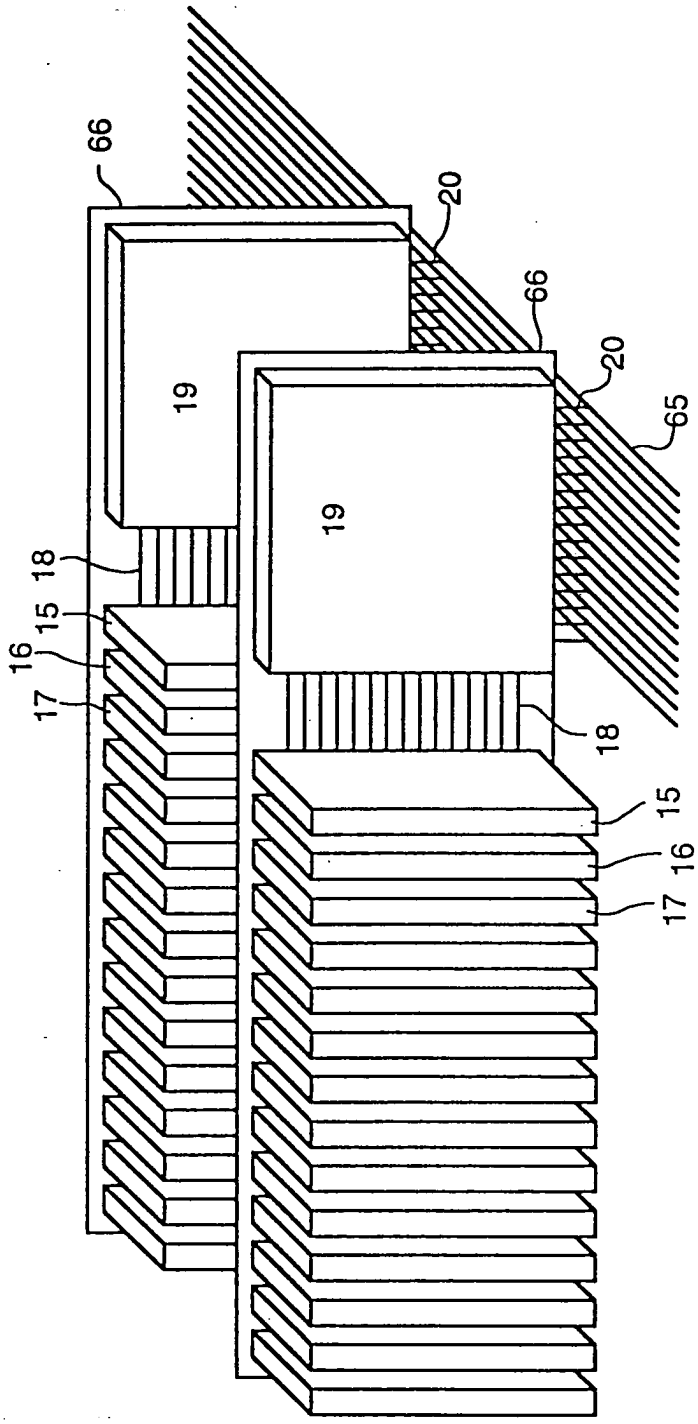


FIG_5

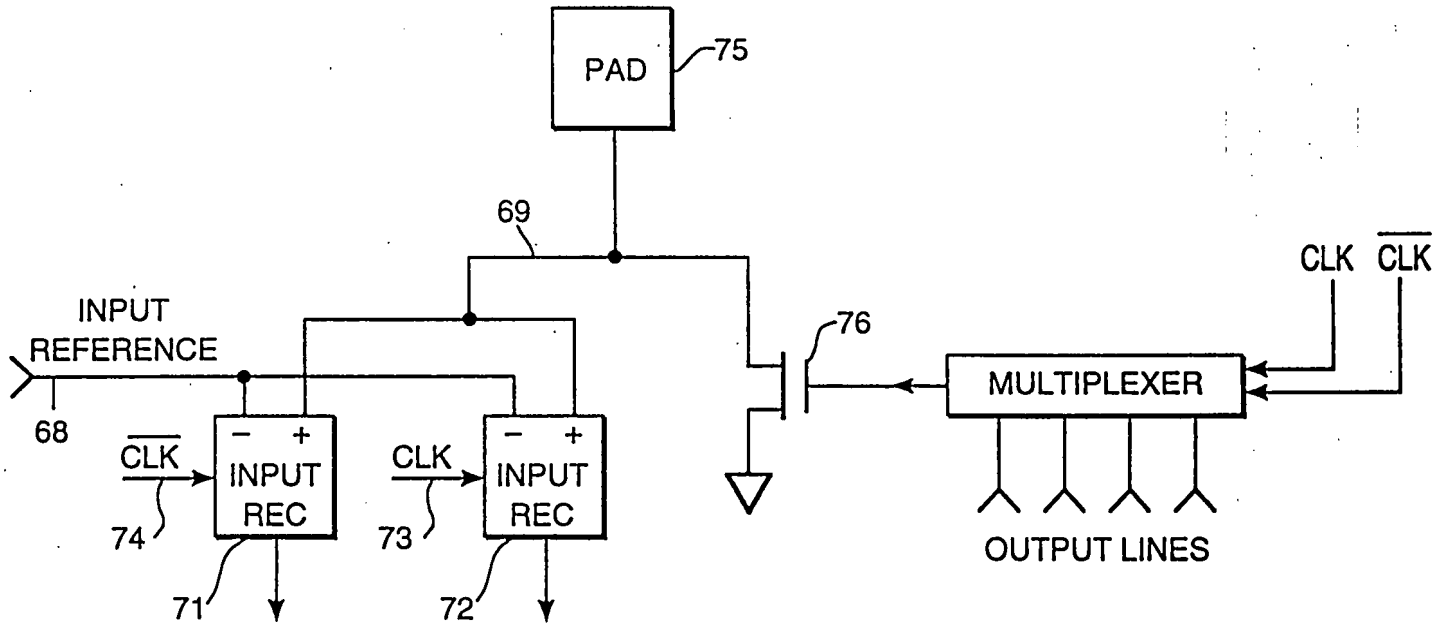

PAD
75
69
CLK
CLK
INPUT
REFERENCE
76
MULTIPLEXER
68
CLK
INPUT
REC
CLK
INPUT
REC
74
73
71
72
OUTPUT LINES

FIG_10